IN THE CLAIMS:

Please cancel Claims 2-4, without prejudice to or disclaimer of the subject matter recited therein.

Please add Claim 12.

Please amend Claims 1, 5-9 and 10-11 as follows:

LISTING OF CURRENT CLAIMS

1. (Currently Amended) An integrated circuit (IC) structure utilized in a standard cell, comprising:

a substrate including pluralities of circuit elements; and

m metal layers, which are disposed on said substrate and utilized as connection layout for circuit elements, wherein each metal layer further including an isolation layer for electrical isolation among metal layers;

said structure is characterized in that one terminal of at least one circuit element is arranged with a circuit passageway, said circuit passageway extends from said substrate to n metal layers such that any connection line in each metal layer can be connected with said terminal by said circuit passageway, wherein n is larger than 1 and n is less than m+1, wherein said circuit passageway is formed by pluralities of metal layers and pluralities of vias, said structure including an upper metal layer overlying said metal layers, fewer than all of said pluralities of vias being connected to said upper metal layer, a remainder of said pluralities of vias being positioned for connection to said upper metal layer during a subsequent reworking of said structure.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The IC structure of claim 1, wherein said standard cell ~~can be~~ is assembled as an intellectual property element.

6. (Currently Amended) The IC structure of claim 1, wherein said standard cell ~~can be~~ is assembled as an intellectual property element library.

7. (Currently Amended) An integrated circuit (IC) layout design method utilized for connection of elements in a standard cell, wherein said IC comprises a substrate, said substrate further including pluralities of circuit elements; and m metal layers disposed on said substrate, which are utilized as a connection layout for circuit elements, wherein each metal layer further including an isolation layer for electrical isolation among said metal layers; said IC layout design method comprising the following steps:

arranging [[a]] pluralities of circuit passageway at one terminal of a circuit element, said pluralities of circuit ~~passageway extends~~ passageways extending from said substrate through at least two of said metal layers; ~~and~~

connecting ~~a line, which is~~ pluralities of lines which are required to be electrically connected to said terminal, to said terminal by connecting said ~~line~~ lines to said circuit ~~passageway~~ passageways;

forming an upper metal layer overlying the pluralities of circuit passageways, said upper metal layer being connected to fewer than all of the pluralities of circuit passageways;

testing said circuit element to identify a desired modification; and

modifying said circuit element by connecting said upper metal layer to one of said pluralities of circuit passageways.

8. (Currently Amended) The IC layout design method of claim 7, wherein at least one of said pluralities of circuit passageways ~~said circuit passageway~~ connects through two metal layers.

9. (Currently Amended) The IC layout design method of claim 7, wherein at least one of said pluralities of circuit passageways ~~said circuit passageway~~ connects through three metal layers.

10. (Currently Amended) The IC layout design method of claim 7, wherein said standard cell ~~can be~~ is connected to an intellectual property element.

11. (Currently Amended) The IC layout design method of claim 7, wherein said standard cell ~~can be~~ is connected to an intellectual property element library.

12. (New) The IC layout design method of claim 7, further comprising reserving said upper metal layer exclusively for modification during a subsequent reworking of said circuit element.